Design Studies for an ASIC Implementation of an Optical OFDM Transceiver

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Abstract *We designed at the register-transfer-level the DSP circuits for a 21.8 Gb/s QPSK-OFDM transceiver, and carried out synthesis and simulations assessing performance, power consumption and chip area, to determine their suitability for low-cost optical interconnects.*

Introduction

High-order multi-carrier modulation formats such as QPSK- or QAM-OFDM [1] are promising approaches to implement the high-capacity optical interconnects required in data centre and high performance computing networks. Proof-of-principle real-time OFDM transmitters [2,3], receivers [4] and transceivers [5] operating at multi-gigabit per second data rates have recently been demonstrated using field programmable gate arrays. However, power consumption must be kept as low as possible, to minimise environmental impact and to avoid escalating operating costs [6], making it necessary to implement the OFDM transceiver DSP and DAC/ADC in application specific integrated circuit (ASIC) form.

We carried out register-transfer-level ASIC design studies assessing the feasibility of using OFDM technology for low-cost, low-power optical interconnects. Key components of a 50 channel, 21.8 Gb/s QPSK-OFDM transceiver were synthesized for a commercial 65nm standard-cell library using the Synopsys Design Compiler [7]. Simulations of the DSP circuits and optical link were performed to assess the dependence of the received signal quality on the resolution of the discrete Fourier transform (DFT) used to demultiplex the channels, and to investigate power consumption and chip area trade-offs for a wide variety of DFT algorithms and implementations.

System configuration

The transceiver design is shown in Fig.1. The incoming bit stream is mapped into QPSK symbols, then fed to a 10-bit 128 point inverse DFT. The system uses the discrete multi-tone (DMT) modulation format [8], in which 50 channels are used to carry data. The remaining 14 channels have zero input to achieve x1.28 oversampling. The time domain signal is then clipped and passed to a 6-bit DAC to convert it into an analogue signal, used, with a DC bias added, to drive an optical intensity modulator. Following direct-detection, the DSP at the receiver converts the incoming serial samples of an 8-bit ADC into parallel and feeds them to an *n*-bit DFT, following which the data-carrying channels are decoded. The DAC and ADC operate at a sampling rate of 28 GSamples/s and the raw data-rate of the OFDM signal is 21.8 Gb/s.

Currently, our transceiver simulations assume synchronisation with a single clock [5]. Further work is planned to develop receiver synchronisation circuits.

We explored a wide space of possible options for DFT algorithms and generated

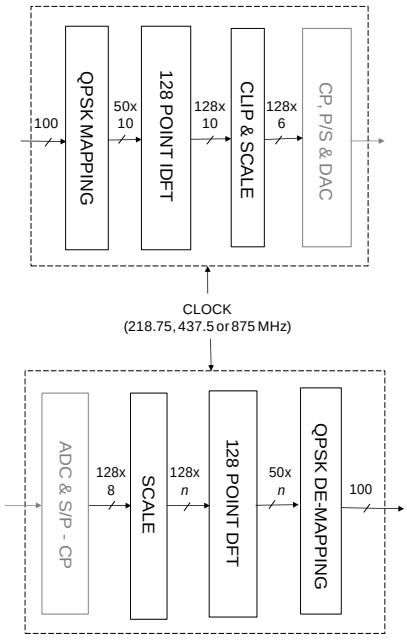

Fig. 1 Top: Transmitter design. Bottom: Receiver design. (CP – cyclic prefix, P/S – parallel-to-serial, S/P – serial-to-parallel,)

hardware implementations of them together with the other DSP components (those shown as black blocks in Fig. 1) as described in the next section.

ASIC power consumption and area

When implementing the discrete Fourier transform (DFT) and its inverse (IDFT) in hardware, there are many different algorithmic and architectural options to choose from. This means that there are many feasible implementations, each with different cost and throughput characteristics. We used the Spiral hardware generation framework [9] to automatically explore a range of register-transfer-level IDFT and DFT implementations in Verilog, and we evaluated each in the context of the proposed transmitter and receiver.

For this study, we generated twenty different IDFT and DFT implementations (with 10 bit and 14 bit fixed point data types, respectively). All designs are based on the Iterative Cooley-Tukey FFT algorithm with varying radices [10]. The designs we consider process either 32, 64, or 128 samples per cycle, and thus must be clocked at 875, 437.5, or 218.75 MHz (respectively) in order to meet the throughput requirement of 28 Gsamples/s. To meet our OFDM performance target, each design must perform approximately 10^{12} fixed point operations per second. The designs that process more samples per cycle have a higher area but are clocked at a lower frequency and thus consume less power. This allows a tradeoff between power consumption and area.

We used Synopsys Design Compiler Ultra [7] to synthesize and characterize the tradeoff between power and area across the transmitter and receiver design space. We constructed transceivers from each generated IDFT and DFT implementation by integrating appropriate modules for QPSK mapping, de-mapping, and clipping/scaling. Then, we synthesized each design for a commercial 65nm standard-cell library.

Fig. 2 shows Design Compiler's reported area and power consumption for each design. Each point on the graph indicates the power (y-axis) and area (x-axis) of a single implementation of the transmitter or receiver. The solid lines indicate the Pareto-optimal set of designs (the set of designs that give the best tradeoff between power and area). The transmitter's Pareto-optimal set contains five designs, ranging from 0.72 mm^2 and 0.44 W to 0.95 mm^2 and 0.17 W. The receiver's Pareto-optimal set contains three designs ranging from 1.14 mm^2 and 0.73 W to 1.35 mm^2 and 0.24 W.

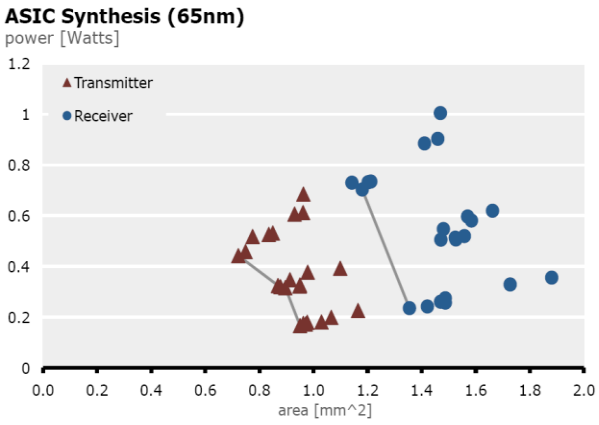

Fig. 2 Power (y-axis) and area (x-axis) for each synthesized transmitter and receiver.

Typically, power is the most critical constraint within the system, so one would choose the lowest/rightmost design from the Pareto-optimal set. However, if the system area is constrained, a smaller (yet higher power) design could be selected. The most power-efficient transmitter consumes 7.6 mW/Gb/s, while the most power-efficient receiver consumes 10.7 mW/Gb/s.

In both the transmitter and receiver, the most power-efficient designs process 128 samples per cycle at 218.75 MHz, while the most area-efficient designs process 32 samples per cycle at 875 MHz. For these architectures, the mixed radix Cooley-Tukey FFT algorithm has lowest cost when radices 8 and 16 are used. Simpler algorithms, such as the commonly-seen radix 2 FFT have higher computational cost and correspond to the least efficient points seen on the graph.

Receiver DFT resolution

Next, we assessed the impact of varying the DFT resolution on the received signal quality. The inverse DFT in the transmitter used a 10 bit precision mixed radix Cooley-Tukey FFT algorithm with radices 8 and 16 as used in our previous work [2], and the precision of the DFT core in the receiver, using the same algorithm, was varied over the range n = 10 to 32 bits. The register-transfer-level transceiver designs, were tested in a Verilog simulation test bench. The input stimulus was a 2^{15} de Bruijn sequence, passed through the IDFT, the output of which was scaled to n bits and fed to the n-bit DFT. Figs. 3 and 4 show the error vector magnitudes (EVM) [11] of the channels at the input to the QPSK de-mapping block for different DFT resolutions. Increasing the resolution reduces the EVM from -11 dB for 10 bits to -35 dB for

32 bits. The 14-bit DFT was found to give a good tradeoff between performance (EVM < -30 dB) and resources, and was used in the optical link simulations, described in the next section.

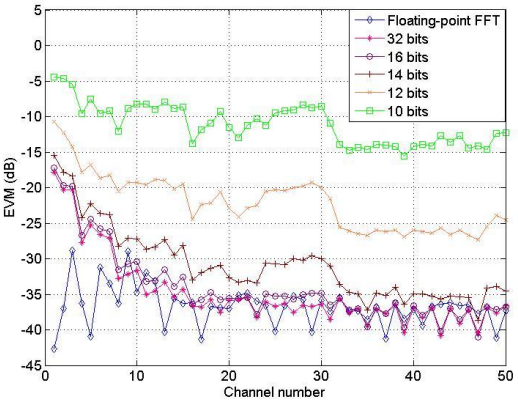

Fig. 3 Received signal error vector magnitudes for a range of DFT resolutions.

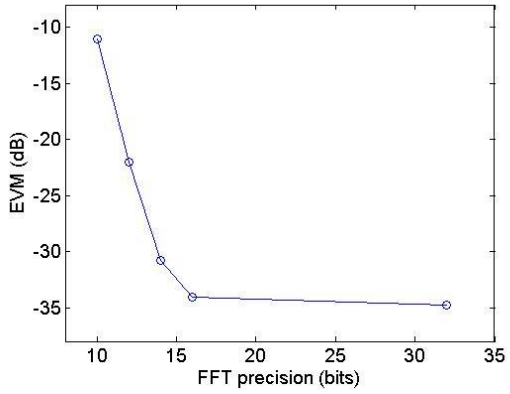

Fig. 4 Received signal error vector magnitude versus receiver DFT resolution (averaged across all 50 channels).

Optical interconnect simulation

The transmitter and receiver DSP designs were tested in simulations of a 300m SMF-based interconnect. The operation of the DAC, ADC, S/P and P/S blocks, and optical components (CW laser, linear intensity modulator, fibre and square-law photodetector) were simulated using Matlab. DAC/ADC and DFT quantisation noise were assumed to be the dominant sources of noise. Fig**.** 5 shows the received signal scatter diagram and EVM values, which were lower than -20 dB for all 50 channels in the received signal, indicating error-free operation would be expected with this system design.

Conclusions

We designed and synthesized 28 GSa/s DSP circuits for a 21.8 Gb/s QPSK-OFDM transceiver, and carried out simulations assessing performance, power consumption and chip area, to determine their suitability for optical interconnects for data centre and high performance computing applications. Based on synthesis for commercial 65nm standard-cell libraries, minimum power consumption of the DFTs, QPSK (de)mapping and clipping/scaling circuits was determined to be 0.41 W in total. This contributes around 18 mW/Gb/s to the power consumption of the OFDM transceiver. This is in addition to the power requirements of the synchronization circuits, and also the DAC and ADC, discussed in detail in e.g. [12]. Optical interconnect simulations using this transceiver design predicted error vector magnitude values lower than -20 dB, indicating error-free operation. Future work extending the design to 16QAM is planned.

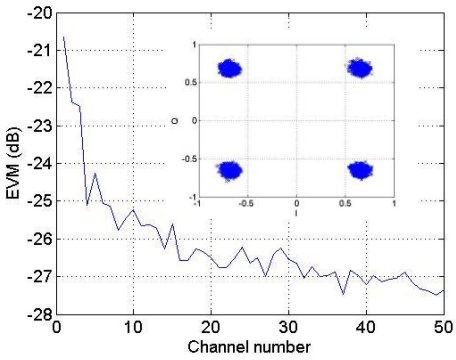

Fig. 5 Optical transmission simulation results. Inset: Received signal constellations for all 50 sub-channels.

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